

## AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph which begins on page 4, line 27 as follows:

The first tap delay line 204, and the register 216, ~~and the second tap delay line 230~~ act as a timing circuitry 255 to measure the Phase0 output {208} high time. The second tap delay line 230 acts as the second timing circuitry 260 to measure ~~and~~ the Phase1 output 244 high time, which is the same as Phase0 low time, of the clock splitter 210.